Appl. No. 10/600,878
Stmt. Subst. Int. dated Aug. 11, 2006
Reply to Examiner's Interview Summary of 7/20/06

Listing of Allowed Claims

This listing of claims reflects a current status of the claims in the instant application subsequent to an Examiner's Amendment and replaces all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Previously Presented): A programmable weak write test mode (PWWTM) bias generator for weak write test mode (WWTM) testing of a static random access memory (SRAM) comprising:

a generator circuit that generates an output signal at an output of the PWWTM bias generator, the output signal being a logic high signal in a default mode, and the output signal being a bias voltage having a selectable magnitude when in a WWTM, the selectable magnitude taking on a selectable one of a plurality of values different from a magnitude of the logic high signal.

Claim 2 (Original): The PWWTM bias generator of Claim 1, wherein the generated output signal biases a gate of a weak write pull-down transistor of a write driver in the SRAM.

Claim 3 (Original): The PWWTM bias generator of Claim 1, further comprising a mode select input that controls a selection between the WWTM and the default mode, a first supply voltage, a second supply voltage, and a set of selection inputs that control the selectable magnitude of the generated bias voltage in WWTM, wherein the second supply voltage is less than the first supply voltage, the second supply voltage optionally being zero volts or a ground voltage.

Claim 4 (Original): The PWWTM bias generator of Claim 3, wherein when in the default mode, the logic high signal is approximately equal to the first supply voltage, the default mode logic high signal being actively maintained when the PWWTM bias generator output is connected to a load.

Claim 5 (Previously Presented): The PWWTM bias generator of Claim 3, wherein the generator circuit comprises:

an array of transistors connected such that a source of each array transistor is connected to the first supply voltage, a drain of each array transistor is connected to the PWWTM bias generator output, and a gate of each array transistor except for a gate of a last array transistor is connected to a different selection input of the set of selection inputs, the gate of the last array transistor being connected to the mode selection input;

a pull-down transistor connected between the PWWTM bias generator output and the second supply voltage, and

a gate bias circuit connected between the mode select input and a gate of the pull-down transistor,

wherein the array transistors are p-type metal oxide semiconductor (PMOS) transistors that function to pull up the generated signal when in an ON state, the pull-down transistor being an n-type metal oxide semiconductor (MNOS) transistor that functions to pull down the generated signal to the second supply voltage when in the ON state.

Claim 6 (Original): A programmable weak write test mode (PWWTM) bias generator for static random access memory (SRAM) weak write test mode (WWTM) testing comprising:

an array of transistors connected in parallel between a first supply voltage and an output of the PWWTM bias generator;

a first pull-down transistor connected between the PWWTM bias generator output and a second supply voltage; and

a gate bias circuit that biases the first pull-down transistor connected between a mode select input and a gate of the first pull-down transistor,

wherein while in a default mode when WWTM is not active, an output signal at the PWWTM bias generator output is a logic high level signal, and

wherein while WWTM is active, the output signal at the PWWTM bias generator output is a bias voltage having a selectable magnitude.

Claim 7 (Original): The PWWTM bias generator of Claim 6, wherein the transistors of the array are p-type metal oxide semiconductor (PMOS) array transistors, the first pull-down transistor being an n-type metal oxide semiconductor (NMOS).

Claim 8 (Original): The PWWTM bias generator of Claim 6, wherein the transistors of the array are further connected to a set of selection inputs, a gate of each array transistor of the array being connected to a different selection input of the set except for a last array transistor, a gate of the last array transistor being connected to the mode select input, wherein each of the array transistors is individually selectable and individually activatable, such that a particular selection and activation of the array transistors selects a particular magnitude of the selectable magnitudes of the bias voltage.

Claim 9 (Original): The PWWTM bias generator of Claim 8, wherein a particular magnitude selection comprises selecting one or more array transistors such that there are more selectable magnitudes than there are array transistors in the array.

Claim 10 (Original): The PWWTM bias generator of Claim 6, wherein at least one array transistors of the array has a transistor size that differs from at least one other array transistor.

Claim 11 (Original): The PWWTM bias generator of Claim 6, wherein the mode select input controls a selection between the WWTM and the default mode, and wherein the second supply voltage is less than the first supply voltage, the second supply voltage optionally being zero volts or a ground voltage.

Claim 12 (Original): The PWWTM generator of Claim 6, wherein when in the default mode, the logic high level signal has a voltage level approximately equal to the first supply voltage, the default mode logic high level signal being actively maintained when the programmable WWTM bias generator output is connected to a load.

Claim 13 (Original): The PWWTM bias generator of Claim 6, wherein the gate bias circuit comprises a second pull-down transistor connected between the first pull-down transistor gate and the second supply voltage, a p-type transistor connected to the first pull-down transistor gate, and an inverter connected between the mode select input and respective gates of the p-type transistor and the second pull-down transistor.

Claim 14 (Original): The PWWTM bias generator of Claim 13, wherein the p-type transistor is further connected to the first supply voltage.

Claim 15 (Original): The PWWTM bias generator of Claim 13, wherein the gate bias circuit further comprises an n-type transistor connected to the p-type transistor that also connects to the first pull-down transistor gate, the p-type transistor and the n-type transistor being further connected to the PWWTM bias generator output, a gate of the n-type transistor being further connected to the mode select input.

Claim 16 (Original): A weak write test mode (WWTM)-enabled static random access memory (SRAM) system comprising:

an SRAM array having a weak write pull-down transistor in a write driver; and

means for biasing the weak write pull-down transistor with a bias voltage, the bias voltage having a voltage equivalent to a logic high level of the SRAM in a default mode when the WWTM is not active, the bias voltage having a selectable magnitude when the WWTM is active.

Claim 17 (Original): The WWTM-enabled SRAM system of Claim 16, wherein the selectable magnitude of the bias voltage compensates for variability in strength of the weak write pull-down transistor, such that sensitivity of the WWTM to sizing of the weak write pull-down transistor is reduced.

Claim 18 (Original): The WWTM-enabled SRAM system of Claim 16, wherein the means for biasing comprises a programmable WWTM (PWWTM) bias generator circuit that comprises:

an array of transistors connected in parallel between a first supply voltage and an output of the PWWTM bias generator;

a generator pull-down transistor connected between the PWWTM bias generator output and a second supply voltage;

a gate bias circuit connected between a mode select input and a gate of the generator pull-down transistor, the gate bias circuit biasing the generator pull-down transistor; and

a set of selection inputs, a gate of each array transistor of the array being connected to a different selection input of the set except for a last array transistor, the gate of the last array transistor being connected to the mode select input,

wherein the logic high magnitude bias voltage in the default mode insures that the weak write pull-down transistor of the write driver is biased to an ON state.

Claim 19 (Original): The programmable WWTM-enabled SRAM system of Claim 18, wherein the selectable magnitude of the bias voltage is selected by asserting one or more of the selection inputs of the set that activate respective one or more array transistors of the array.

Claim 20 (Previously Presented): A method of driving a weak write test mode (WWTM)-equipped static random access memory (SRAM) comprising:

generating a bias voltage and applying the generated bias voltage to a gate of a weak write pull-down transistor of a write driver while conducting a WWTM test of the SRAM; and

generating a logic high output signal and applying the logic high output signal to the gate of the weak write pull-down transistor while in a default mode when not conducting the WWTM test of the SRAM,

wherein the bias voltage has a selectable magnitude different from a magnitude of the logic high output signal.

Claim 21 (Previously Presented): The method of driving of Claim 20, wherein the bias voltage selectable magnitude modulates an effective ON state resistance of the weak write pull-down transistor, such that a threshold of a detected memory cell failure is adjustable by selecting a magnitude from among a plurality of selectable magnitudes.

Claim 22 (Original): The method of driving of Claim 21, wherein the adjustable threshold is used to account for manufacturing related variations in the ON state resistance of the weak write pull-down transistor.

Claim 23 (Original): The method of driving of Claim 20, wherein the logic high output signal has a voltage that is sufficient to activate an ON state of the weak write pull-down transistor, such that the weak write pull-down transistor is turned ON when the SRAM is operating in the default mode.

Claim 24 (Original): The method of driving of Claim 20, wherein the application of the logic high output signal improves a write margin of memory cells in the SRAM.